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the compileultracommand consult the Design Compiler User Guide (dc-user-guide.pdf) or use `man compileultra` at the DC shell prompt.

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Run the following command and take a look at the output. DC will attempt to synthesize your design while still meeting the constraints. DC considers two RTL-to-Gates Synthesis using Synopsys Design Compiler

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CS250 Tutorial 5 (Version 091210b) September 12, 2010 Yunsup Lee. In this tutorial you will gain experience using Synopsys Design Compiler (DC) to perform hardware synthesis. A synthesis tool takes an RTL hardware description and a standard cell library as input and produces a gate-level netlist as output. The resulting gate-level netlist is a completely structural description with standard cells only at the leaves of the design.

*RTL-to-Gates Synthesis using Synopsys Design Compiler*

The following command tells # the tool that the pin named clk is the clock and that the desired clock # period is 1 nanosecond. dc\_shell-topo> create\_clock clk -name ideal\_clock1 -period 1 # The compile\_ultra command begins the actual synthesis process that # transforms your design into a gate-level netlist.

*RTL-to-Gates Synthesis using Synopsys Design Compiler*

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Logic synthesis has become a fundamental component of the ASIC design flow, and Logic Synthesis Using Synopsys® has been written for all those who dislike reading manuals but who still like to learn logic synthesis as practised in the real world. The primary focus of the book is Synopsys Design Compiler®: the leading synthesis tool in the EDA marketplace. The book is specially organized to assist designers accustomed to schematic capture based design to develop the required expertise to effectively use the Compiler. Over 100 'classic scenarios' faced by designers using the Design Compiler have been captured and discussed, and solutions provided. The scenarios are based both on personal experiences and actual user queries. A general understanding of the problem-solving techniques provided will help the reader debug similar and more complicated problems. Furthermore, several examples and dc-shell scripts are provided. Specifically, Logic Synthesis Using Synopsys® will help the reader develop a better understanding of the synthesis design flow, optimization strategies using the Design Compiler, test insertion using the Test Compiler®, commonly used interface formats such as EDIF and SDF, and design re-use in a synthesis-based design methodology. Examples have been provided in both VHDL and Verilog. Audience: Written with CAD engineers

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in mind to enable them to formulate an effective synthesis-based ASIC design methodology. Will also assist design teams to better incorporate and effectively integrate synthesis with their existing in-house design methodology and CAD tools.

Advanced ASIC Chip Synthesis: Using Synopsys® Design Compiler® and PrimeTime® describes the advanced concepts and techniques used for ASIC chip synthesis, formal verification and static timing analysis, using the Synopsys suite of tools. In addition, the entire ASIC design flow methodology targeted for VDSM (Very-Deep-Sub-Micron) technologies is covered in detail. The emphasis of this book is on real-time application of Synopsys tools used to combat various problems seen at VDSM geometries. Readers will be exposed to an effective design methodology for handling complex, sub-micron ASIC designs. Significance is placed on HDL coding styles, synthesis and optimization, dynamic simulation, formal verification, DFT scan insertion, links to layout, and static timing analysis. At each step, problems related to each phase of the design flow are identified, with solutions and work-arounds described in detail. In addition, crucial issues related to layout, which includes clock tree synthesis and back-end integration (links to layout) are also discussed at length. Furthermore, the book contains in-depth discussions on the basics of Synopsys technology libraries and HDL coding styles, targeted towards optimal synthesis solutions. Advanced ASIC Chip Synthesis: Using Synopsys® Design Compiler® and PrimeTime® is intended for anyone who is involved in the ASIC design methodology, starting from RTL synthesis to final tape-out. Target audiences for this book are practicing ASIC design engineers and graduate students undertaking advanced courses in ASIC chip design and DFT techniques. From the Foreword: `This book, written by Himanshu Bhatnagar, provides a comprehensive overview of the ASIC design

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flow targeted for VDSM technologies using the Synopsis suite of tools. It emphasizes the practical issues faced by the semiconductor design engineer in terms of synthesis and the integration of front-end and back-end tools. Traditional design methodologies are challenged and unique solutions are offered to help define the next generation of ASIC design flows. The author provides numerous practical examples derived from real-world situations that will prove valuable to practicing ASIC design engineers as well as to students of advanced VLSI courses in ASIC design'. Dr Dwight W. Decker, Chairman and CEO, Conexant Systems, Inc., (Formerly, Rockwell Semiconductor Systems), Newport Beach, CA, USA.

This book contains the papers presented at the 9th International Workshop on Field Programmable Logic and Applications (FPL'99), hosted by the University of Strathclyde in Glasgow, Scotland, August 30 – September 1, 1999. FPL'99 is the ninth in the series of annual FPL workshops. The FPL'99 programme committee has been fortunate to have received a large number of high-quality papers addressing a wide range of topics. From these, 33 papers have been selected for presentation at the workshop and a further 32 papers have been accepted for the poster sessions. A total of 65 papers from 20 countries are included in this volume. FPL is a subject area that attracts researchers from both electronic engineering and computer science. Whether we are engaged in research into soft hardware or hard software seems to be primarily a question of perspective. What is unquestionable is that the interaction of groups of researchers from different backgrounds results in stimulating and productive research. As we prepare for the new millennium, the premier European forum for researchers in field programmable logic remains the FPL workshop. Next year the FPL series of workshops will celebrate its tenth anniversary. The contribution of so many overseas researchers has been a particularly attractive feature of these events, giving them a truly international perspective, while the informal and convivial atmosphere that pervades the workshops

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have been their hallmark. We look forward to preserving these features in the future while continuing to expand the size and quality of the events.

After a brief introduction to low-power VLSI design, the design space of ASIP instruction set architectures (ISAs) is introduced with a special focus on important features for digital signal processing. Based on the degrees of freedom offered by this design space, a consistent ASIP design flow is proposed: this design flow starts with a given application and uses incremental optimization of the ASIP hardware, of ASIP coprocessors and of the ASIP software by using a top-down approach and by applying application-specific modifications on all levels of design hierarchy. A broad range of real-world signal processing applications serves as vehicle to illustrate each design decision and provides a hands-on approach to ASIP design. Finally, two complete case studies demonstrate the feasibility and the efficiency of the proposed methodology and quantitatively evaluate the benefits of ASIPs in an industrial context.

Very Large Scale Integration (VLSI) Systems refer to the latest development in computer microchips which are created by integrating hundreds of thousands of transistors into one chip. Emerging research in this area has the potential to uncover further applications for VLSI technologies in addition to system advancements. Design and Modeling of Low Power VLSI Systems analyzes various traditional and modern low power techniques for integrated circuit design in addition to the limiting factors of existing techniques and methods for optimization. Through a research-based discussion of the technicalities involved in the VLSI hardware development process cycle, this book is a useful resource for researchers, engineers, and graduate-level students in computer science and engineering.

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Designed for senior electrical engineering students, this textbook explores the theoretical concepts of digital signal processing and communication systems by presenting laboratory experiments using real-time DSP hardware. The experiments are designed for the Texas Instruments TMS320C6701 Evaluation Module or TMS320C6711 DSK but can easily be adapted to other DSP boards. Each chapter begins with a presentation of the required theory and concludes with instructions for performing experiments to implement the theory. In the process of performing the experiments, students gain experience in working with software tools and equipment commonly used in industry.

This book constitutes the refereed proceedings of the 13th International Conference on Compiler Construction, CC 2004, held in Barcelona, Spain, in March/April 2004. The 19 revised full papers presented together with the abstract of an invited talk were carefully reviewed and selected from 58 submissions. The papers are organized in topical sections on program analysis, parsing, loop analysis, optimization, code generation and backend optimizations, and compiler construction.

This book makes powerful Field Programmable Gate Array (FPGA) and reconfigurable technology accessible to software engineers by covering different state-of-the-art high-level synthesis approaches (e.g., OpenCL and several C-to-gates compilers). It introduces FPGA technology, its programming model, and how various applications can be implemented on FPGAs without going through low-level hardware design phases. Readers will get a realistic sense for problems that are suited for FPGAs and how to implement them from a software designer's point of view. The authors demonstrate that FPGAs and their programming model reflect the needs of stream processing problems much better than traditional CPU or GPU architectures, making them well-suited for a wide variety of systems, from embedded systems performing sensor processing to

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large setups for Big Data number crunching. This book serves as an invaluable tool for software designers and FPGA design engineers who are interested in high design productivity through behavioural synthesis, domain-specific compilation, and FPGA overlays. Introduces FPGA technology to software developers by giving an overview of FPGA programming models and design tools, as well as various application examples; Provides a holistic analysis of the topic and enables developers to tackle the architectural needs for Big Data processing with FPGAs; Explains the reasons for the energy efficiency and performance benefits of FPGA processing; Provides a user-oriented approach and a sense for where and how to apply FPGA technology.

Advanced ASIC Chip Synthesis: Using Synopsys® Design Compiler® Physical Compiler® and PrimeTime®, Second Edition describes the advanced concepts and techniques used towards ASIC chip synthesis, physical synthesis, formal verification and static timing analysis, using the Synopsys suite of tools. In addition, the entire ASIC design flow methodology targeted for VDSM (Very-Deep-Sub-Micron) technologies is covered in detail. The emphasis of this book is on real-time application of Synopsys tools, used to combat various problems seen at VDSM geometries. Readers will be exposed to an effective design methodology for handling complex, sub-micron ASIC designs. Significance is placed on HDL coding styles, synthesis and optimization, dynamic simulation, formal verification, DFT scan insertion, links to layout, physical synthesis, and static timing analysis. At each step, problems related to each phase of the design flow are identified, with solutions and work-around described in detail. In addition, crucial issues related to layout, which includes clock tree synthesis and back-end integration (links to layout) are also discussed at length. Furthermore, the book contains in-depth discussions on the basis of Synopsys technology libraries and HDL coding styles, targeted towards optimal synthesis solution. Target audiences for this book

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are practicing ASIC design engineers and masters level students undertaking advanced VLSI courses on ASIC chip design and DFT techniques.

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